In the Claims

1. (Original) An apparatus comprising:

a first solid-state memory die;

a second solid-state memory die; and

a controller sensing one or more operating parameters for the first and the second solid-state memory die and making intelligent decisions on where to write data, based on the operating parameters.

2. (Original) The apparatus of claim 1 wherein the first and second solid-state memory die comprises flash memory, MRAM, SRAM, DRAM, FRAM, or polymer memory.

3. (Original) The apparatus of claim 1 wherein the operating parameters comprise temperature, current draw, or access time.

4. (Original) The apparatus of claim 1 further comprising a database storing known operating models for the first and the second die.

5. (Original) The apparatus of claim 1 further comprising a database storing known operating models for the first and the second solid-state memory die, and wherein the controller senses one or more operating parameters for the first and the second solid-state memory die and accesses the known operating models for the first and the second die and makes intelligent decisions on where to write data, based on the operating parameters and the known operating models.

6. (Original) The apparatus of claim 1 further comprising a File Access Table (FAT) storing available memory locations within the first and the second die.

7. (Original) An apparatus comprising:

a performance model database storing historical operating parameters for a plurality of memory die;

a processor/test controller having operating parameters for the plurality of memory die as an input and outputting optimal storage locations;

a controller having data as an input and outputting the data destined to be written to a first memory location; and

a hardware re-router having the optimal storage locations as an input along with the data, and re-routing the data, based on the optimal storage locations.

8. (Original) The apparatus of claim 7 wherein the memory die comprises memory taken from the group consisting of flash memory, MRAM, SRAM, DRAM, FRAM, and polymer memory.

9. (Original) The apparatus of claim 7 wherein the operating parameters comprise operating parameters taken from the group consisting of temperature, current draw, access times, and whether the memory die is functional.

Claims 10-15 have been cancelled.